REMARKS

The Examiner is thanked for the thorough examination of the present application. The Non-Final Office Action mailed March 20, 2007, however, tentatively rejected all examined claims 1-9, 11, and 13-22. Applicant respectfully requests reconsideration of the rejections for at least the reasons set forth below.

Rejections under 35 U.S.C. 103

The Office Action rejected claims 1, 2, 9, 13, 15, 19, and 21 under 35 U.S.C. 103(a) as allegedly anticipated by Fujii et al. (USP 5,644,158) in view of Jeon (US Pat. Pub. 2003/0194853), and evidenced by Chao (USP 4906589) and Weber et al. (USP 5,075,641). Applicant respectfully traverses this rejection.

In order for a claim to be properly rejected under 35 U.S.C. §103, the teachings of the prior art reference must suggest all features of the claimed invention to one of ordinary skill in the art. *See, e.g., In re Dow Chemical*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988); *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

Turing now to claim 1, independent claim 1 recites:

> 1. A method for treating a gate structure comprising a high-K gate dielectric stack to reduce interface states between a high-k gate dielectric and a gate electrode comprising the steps of:
>
> providing a gate dielectric layer stack comprising a high-k gate dielectric over a semiconductor substrate;
>
> forming a gate electrode layer on the gate dielectric layer stack;
>
> lithographically patterning and etching to form a gate structure; and,
>
> ***carrying out at least one plasma treatment of the gate structure following formation of the gate structure, said at least one plasma treatment comprising a plasma***

source gas selected from the group consisting of H_2, N_2, O_2, NH_3, and combinations thereof.

(*Emphasis Added*)

Independent claim 13 recites:

> 13. A method for treating a gate structure comprising a high-K gate dielectric stack to reduce interface states at a high-k gate dielectric/gate electrode interface comprising the steps of:
>
> providing a gate dielectric layer stack comprising at least one high-K dielectric over a semiconductor substrate;
>
> forming a gate electrode layer on the high-k dielectric layer;
>
> lithographically patterning and etching to form a gate structure;
>
> ***carrying out at least one plasma treatment of the gate structure following formation of the gate structure, said at least one plasma treatment comprising a plasma source gas selected from the group consisting of H_2, N_2, O_2, NH_3, and combinations thereof***; and,
>
> annealing the gate structure following the at least one plasma treatment.

(*Emphasis Added*) Independent claims 1 and 13 patently define over the cited art for at least the reasons that the cited art fails to disclose the features emphasized above in each of these claims.

On page 3 of the Office Action, the Examiner alleged that the feature "forming a thin film capacitance layer using a sputtering method" disclosed in the Fujii reference teaches the feature "at least one plasma treatment comprising source gas N2 gate structure following the formation of the gate structure" as recited in the claims 1 and 13. Applicant respectfully disagrees.

As disclosed in FIG. 2 and column 4, lines 1-14, of the Fujii reference, an integrated circuit represented by a transistor comprising gate electrode 6a and diffusion area 6b is first formed by using a regular technique for forming a transistor. An interlayer insulating layer 7 is then formed to cover an integrated circuit area and the oxide layer 5

by using CVD method. Next, a thin-film-type capacitance element 16 is formed on a specific area of the interlayer insulating layer 7 using a sputtering method.

Since the thin-film-type capacitance element 16 in the Fujii reference is not formed following formation of the integrated circuit comprising a transistor but following formation of the interlayer insulating layer 7, the sputtering method for forming the thin-film-type capacitance element 16 is a treatment of the interlayer insulating layer 7 but not of the gate structure.

For at least this reason, Applicant respectfully submits that independent claims 1 and 13 patently define over the teachings of Fujii and the other cited references. In addition, the Jeon reference, the Chao reference and the Weber et al. reference, however, also at least fails to teach the above feature emphasized in claims 1 and 13.

Therefore, the Applicant respectfully asserts that the recited references, either individually or in combination, are legally deficient for the purpose of rendering claims 1, 13 and 21 obvious and the above 103 rejections of claims 1, 13, and 21 are improper and should be removed. Also, since claims 2, 9 and 15 are dependent claims that respectively depend from claim 1 or 13 either directly or indirectly. Applicant respectfully asserts that these claims also are in condition for allowance.

Further, independent claim 21 recites:

> 21. A method for treating a gate structure comprising a high-k gate dielectric stack to improve electric performance characteristics comprising the steps of:
>
> providing a high-k gate dielectric layer over a semiconductor substrate;
>
> forming a gate electrode layer on the high-k gate dielectric layer;
>
> patterning said gate electrode layer and gate dielectric layer to form a gate structure; and

providing a treatment of the gate structure following formation of the gate structure, said treatment selected from the group consisting of a thermal treatment and ***at least one plasma treatment, said treatment reducing interface states between the gate electrode layer and the high-k gate dielectric layer***.

(*Emphasis Added*). Independent claim 21 patently defines over the cited art for at least the reasons that the cited art fails to disclose the features emphasized above in each of these claims.

With regard to claim 21, the Office Action alleged that this claim only rearranges elements recited in claim 1, and therefore is rejected on the same basis as claim 1. As such, and as claim 1 has been distinguished above, Applicant submits that the rejection of claim 21 should be withdrawn for at least the same reason that the rejection of claim 1 should be withdrawn.

As a separate and independent basis for the patentability of all claims, Applicant submits that the combination of Fujii, Jeon, Choa, and Weber is improper, and as such does not render the claims obvious. In this regard, the Office Action combined Choa and Fujii to reject the claims on the solely expressed basis that "Fujii et al's silence shows and [sic] absence of criticality in the method implored, and Choa provides evidence that it is well known and functional to do so" and "it saves time and cost savings to do so." (see e.g., Office Action, p. 3)

This rationale is both incomplete and improper in view of the established standards for rejections under 35 U.S.C. § 103.

In this regard, the MPEP section 2141 states:

> Office policy has consistently been to follow *Graham v. John Deere Co*. in the consideration and determination of obviousness under 35 U.S.C. 103. As quoted above, the four factual inquires enunciated therein as a background for determining obviousness are briefly as follows:
>
> (A) Determining of the scope and contents of the prior art;
>
> (B) Ascertaining the differences between the prior art and the claims in issue;
>
> (C) Resolving the level of ordinary skill in the pertinent art; and
>
> (D) Evaluating evidence of secondary considerations.
>
> …
>
> BASIC CONSIDERATIONS WHICH APPLY TO OBVIOUSNESS REJECTIONS
>
> When applying 35 U.S.C. 103, the following tenets of patent law must be adhered to:
>
> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.
>
> *Hodosh v. Block Drug Co., Inc*., 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

The foregoing approach to obviousness determinations was recently confirmed by the United Stated Supreme Court decision in KSR INTERNATIONAL CO. V. TELEFLEX INC. ET AL. 550 U.S. ___ (2007)(No. 04-1350, slip opinion, p. 2), where the Court stated:

> In Graham v. John Deere Co. of Kansas City, 383 U. S. 1 (1966), the Court set out a framework for applying the statutory language of §103, language itself based on the logic of the earlier decision in Hotchkiss v. Greenwood, 11 How. 248 (1851), and its progeny. See 383 U. S., at 15–17. The analysis is objective:
>
> "Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or nonobviousness of the

> subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., mightbe utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." Id., at 17–18.

Simply stated, the Office Action has failed to at least (1) ascertain the differences between and prior art and the claims in issue; and (2) resolve the level of ordinary skill in the art. Further still, the Office Action seems to point to the FAILURE of Fujii to disclose a certain feature as evidence of another point. This is improper. Certainly an absence of disclosure in an APPLICANT'S specification can be relied upon by the PTO to evidence lack of criticality (because it is deemed an admission against the Applicant's interests). However, the same cannot be relied upon with respect to a third party disclosure. That is, the Examiner cannot apply a lack of disclosure in Fujii as some sort of admission against Applicant. Doing so would allow the Patent Office to cite completely unrelated patents in its rejections (e.g., patents to unrelated inventions would certainly have a failure to disclose relevant material).

For at least these reasons, the rejection that has been formed under 35 U.S.C. § 103 are improper, and should be withdrawn. Applicant also notes that the Examiner relied on the exact same alleged motivation for combining Weber.

For at least the foregoing reasons, the rejections of independent claims 1, 13, and 21 should be withdrawn. As all remaining claims depend from claim 1, 13, or 21, the rejections of all remaining claims should be withdrawn for at least the same reasons.

NOTICE REGARDING CORRESPONDANCE ADDRESS/ATTORNEY

The undersigned wishes to notify the Examiner that the undersigned has received instruction from the Applicant to assume responsibility for the prosecution of this application, and a revocation/power of attorney will be filed shortly. In the meantime, the undersigned respectfully requests that all future communications be directed to the following:

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CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicants respectfully submit that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the pending claims are in condition for allowance.

Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.